REMARKS/ARGUMENTS

The above-identified patent application has been amended and reconsideration and re-examination are hereby requested.

Claims 5 and 9 stand rejected under 35 USC 103.

Claims 5 and 9 point out that each one of the director include a data pipe section having, an input/output interface memory, for receiving data from a source thereof and for returning data to such source; and, a microprocessor for controlling the data pipe section in accordance with information sent thereto from a remote one of the directors, such microprocessor having a CPU and a CPU memory, such ***CPU memory*** having thereon the inbound one of the inbound queue and the outbound queue for storing inbound information passed to such director for processing therein, such information being sent to director from an originating one of the directors; and wherein each one of ***the input/output interface memories*** includes the outbound one of the inbound queue and outbound queue for outbound information being returned to the source through such originating one of the directors after being processed by the microprocessor of such remote one of the directors.

As pointed out in the patent application beginning at paragraph [62]:

Referring now to FIG. 13, the director shown in FIG. 3 is shown in more detail. Thus, the data pipe 38 is shown to include an input/output (I/O) interface, a data pipe/Queue controller as well as the packetizer and depacketizer. Note that the data pipe/queue controller includes an I/O memory and a translation table to be described in more detail below. ***Suffice it to say here that the I/O interface memory does not include a section for an inbound queue for reasons to be described below. The queue for inbound messages are stored in the CPU memory of the director which is to execute the inbound message and hence a "virtual" queue is shown dotted in the I/O interface memory, it being understood that such memory does not store inbound messages producer or consumer indices.***

The microprocessor memory (i.e., the CPU memory) is shown to include in a section thereof an inbound queue. ***It is noted that the microprocessor memory does not include a***

section for an outbound queue for reasons to be described below. The queue for outbound messages are stored in the I/O interface memory of the director which is to execute the inbound message and hence a "virtual" queue is shown dotted in the microprocessor memory, it being understood that such memory is not required to store outbound message's producer or consumer indices.

This is not described in Calvignac (U. S. Patent No. 6,044,079) or in Pierson (USP 2003/0048781) taken either singly or in combination.

New claim 12 points out that the CPU memory has therein ***only*** the inbound one of the inbound queue and the outbound queue and wherein each one of the input/output interface memories includes ***only*** the outbound one of the inbound queue and outbound queue.

In the event a petition for extension of time is required by this paper and not otherwise provided, such petition is hereby made and authorization is provided herewith to charge deposit account No. 05-0889 for the cost of such extension.

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Date

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